TSMC 01-280B


January 5, 2004

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
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Subject: Serial No. 10/686,794 10/16/03

Chia-Ta Hsieh

A FLASH EEPROM WITH FUNCTION BIT BY BIT ERASING

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on January 13, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date 1/13/04

In the article, "A Dual-bit Split-Gate EEPROM (DSG) Cell in Contactless Array for Single-Vcc High Density Flash Memories," by Yale Ma et al., IEDM 94-57, pp. 3.5.1 to 3.5.4, a new source-side injection Dual-bit Split-Gate (DSG) flash EEPROM cell is designed and characterized.

The following two U.S. Patents disclose a triple polysilicon flash EEPROM array having a separate erase gate for each row of floating gates, and methods of manufacturing such an array:

1) U.S. Patent 5,712,179 to Yuan, "Method of Making Triple Polysilicon Flash EEPROM Arrays Having a Separate Erase Gate for Each Row of Floating Gates."
2) U.S. Patent 6,028,336 to Yuan, "Triple Polysilicon Flash EEPROM Arrays Having a Separate Erase Gate for Each Row of Floating Gates, and Methods of Manufacturing Such Arrays."

U.S. Patent 5,677,872 to Samachisa et al., "Low Voltage Erase of a Flash EEPROM System Having a Common Erase Electrode for Two Individual Erasable Sectors," discusses low voltage erase of a flash EEPROM system having a common erase electrode for two individual erasable sectors.

U.S. Patent 5,278,439 to Ma et al., "Self-Aligned Dual-Bit Split Gate (DSG) Flash EEPROM Cell," discloses a DSG EEPROM.

U.S. Patent 6,222,762 to Guterman et al., "Multi-State Memory," discloses a multi-state cell and erase method.

U.S. Patent 6,151,248 to Harari et al., "Dual Floating Gate EEPROM Cell Array with Steering Gates Shared by Adjacent Cells," discloses a EEPROM cell with gates shared by adjacent cells.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761

Form PTO-1449

# INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)



| Docket Number (Optional) | Application Number |
|---|---|
| TSMC-01-280B | 10/686,794 |
| Applicant: Chia-Ta Hsieh | |
| Filing Date: 10/16/03 | Group Art Unit |

## U.S. PATENT DOCUMENTS

| EXAMINER INITIAL | DOCUMENT NUMBER | DATE | NAME | CLASS | SUBCLASS | FILING DATE IF APPROPRIATE |
|---|---|---|---|---|---|---|
| | 5,712,179 | 1/27/98 | Yuan | 437 | 43 | 10/31/95 |
| | 6,028,336 | 2/22/00 | Yuan | 257 | 315 | 8/7/97 |
| | 5,677,872 | 10/14/97 | Samachisa et al. | 365 | 185.14 | 7/8/96 |
| | 5,278,439 | 1/11/94 | Ma et al. | 257 | 319 | 8/29/91 |
| | 6,222,762 | 4/24/01 | Guterman et al. | 365 | 185.03 | 8/7/97 |
| | 6,151,248 | 11/21/00 | Harari et al. | 365 | 185.14 | 6/30/99 |
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## FOREIGN PATENT DOCUMENTS

| | DOCUMENT NUMBER | DATE | COUNTRY | CLASS | SUBCLASS | Translation YES | Translation NO |
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## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

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|---|---|
| | Y. Ma et al., "A Dual-bit Split-Gate EEPROM (DSG) Cell in Contactless Array for Single-Vcc High Density Flash Memories," IEDM 94-57, 1994 IEEE, pp. 3.5.1 to 3.5.4. |
| | |

| EXAMINER | DATE CONSIDERED |
|---|---|
| | |

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant